FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)
A-401	09/914505

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/03040	11 May 2000	11 May 1999

TITLE OF INVENTION

INTERPOLATION CIRCUIT

APPLICANT(S) FOR DO/EO/US

Yukio KOYANAGI

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☒ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☒ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Inventor Information Sheet (Patent Bibliographical Data);
Copies of two Written Opinions (dated February 27, 2001, and June 5, 2001);
[redacted]
Small Entity Statement

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/914505	PCT/JP00/03040	A-401

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**	
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**	
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**	
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
	ENTER APPROPRIATE BASIC FEE AMOUNT =	**$860.00**
	Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	10 - 20 =	0	x $18.00	**$0.00**
Independent claims	4 - 3 =	1	x $80.00	**$80.00**
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**

TOTAL OF ABOVE CALCULATIONS =		**$940.00**
☒ Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.		**$470.00**
SUBTOTAL =		**$470.00**
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +		**$0.00**
TOTAL NATIONAL FEE =		**$470.00**
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**	☒	**$40.00**
TOTAL FEES ENCLOSED =		**$510.00**
	Amount to be: refunded	$
	charged	$

a. ☒ A check in the amount of **$510.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

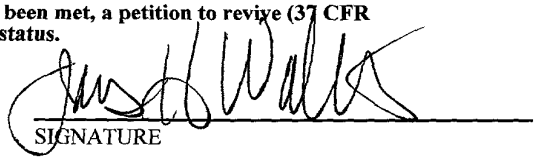
c. ☐ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. _____ A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

James H. Walters
802
DELLETT AND WALTERS
310 S.W. Fourth Avenue, Suite 1101
Portland, Oregon 97204 US
(503) 224-0115



SIGNATURE

James H. Walters

NAME

35,731

REGISTRATION NUMBER

Aug 28, 2001

DATE

INVENTOR INFORMATION

Inventor One Given Name:: Yukio
Family Name:: Koyanagi
Postal Address Line One:: 63-1-205 Isawa-chou
Postal Address Line Two:: Higashiyatsushiro-gun
City:: Yamanashi
Country:: JAPAN
Postal or Zip Code:: 406-0000
City of Residence:: Yamanashi
Country of Residence:: JAPAN
Citizenship Country:: JAPAN

CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 802
Electronic Mail One:: patents@onemain.com

APPLICATION INFORMATION

Title Line One:: INTERPOLATION CIRCUIT
Total Drawing Sheets:: 15
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: A-401
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 802
Registration Number One:: 35731

CONTINUITY INFORMATION

This application is a:: 371 OF
> Application One:: PCT/JP00/03040
Filing Date:: 05-11-2000

PRIOR FOREIGN APPLICATIONS

Foreign Application One:: 11-165745
Filing Date:: 05-11-1999
Country:: JAPAN
Priority Claimed:: Yes

Source:: PrintEFS Version 1.0.1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yukio KOYANAGI

S. N.
International S.N.: PCT/JP00/03040

Filed:
International Filing Date: 11 May 2000

For: INTERPOLATION CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please make the following amendments to this application prior to examination thereof:

In the Claims:

Please amend claim 6 by replacing it with the like numbered claim hereinbelow. A mark up of claim 6 is provided at the end of the amendment to illustrate the changes made for the Examiner.

6. (Amended) The interpolation circuit according to claim 1, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

Add new claims 7-10 as follows:

7. The interpolation circuit according to claim 2, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

8. The interpolation circuit according to claim 3, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

9. The interpolation circuit according to claim 4, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

10. The interpolation circuit according to claim 5, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

In the Drawings:

Please amend FIG. 19 as indicated in red on the drawing sheet attached herewith.

REMARKS

The above amendments to the claims are presented in order to put the multiple dependent claims in non-multiple dependent format. The amendment to FIG. 19 is presented in order to correct a typographical error and is apparent from review of the specification.

Respectfully submitted,

James H. Walters, Reg. No. 35,731

802
DELLETT AND WALTERS
Suite 1101
310 S.W. Fourth Avenue
Portland, Oregon 97204 US
(503) 224-0115
DOCKET: A-401

MARKUP SHEET SHOWING CLAIM AMENDMENTS MADE HEREIN

6. (Amended) The interpolation circuit according to [any one of claims 1 through 5] claim 1, characterized by comprising data appending unit for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

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FIG. 19

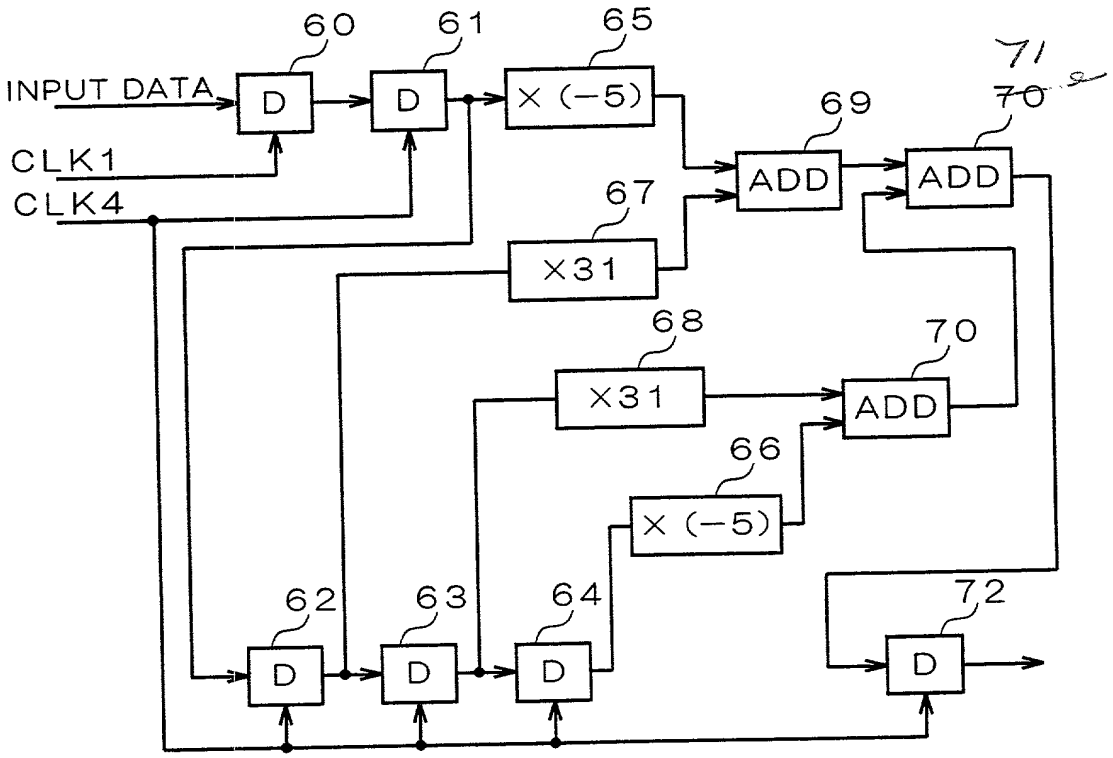
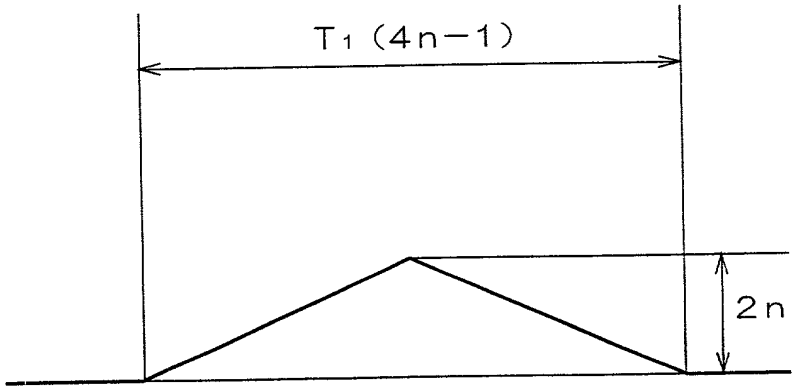


FIG. 20



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DESCRIPTION

INTERPOLATION CIRCUIT

TECHNICAL FIELD

The present invention relates to an interpolation circuit for generating interpolated data from discrete data.

BACKGROUND ART

Conventional CD (Compact Disk) reproducing devices employ a digital-analog converter of the oversampling method. This digital-analog converter performs interpolation operation for digital data discretely input, employing a sinc function or the like. However, this sinc function converges to 0 at $\pm\infty$, and has a shortcoming that if the arithmetic operation is truncated at the finite value, a truncation error occurs in the operation. Generally, a stepwise waveform obtained in the interpolation operation is passed through a low-pass filter, but there is also a drawback that a phase distortion or a distorted output waveform may arise through the low-pass filter.

Particularly, in the above interpolation operation using the sinc function, a method is taken in which the values of the sinc function are stored in a table, and read as needed, or held as the tap coefficients for a digital filter, but this method has a problem that the configuration is complex.

Therefore, an interpolation circuit capable of performing interpolation operation with a simple constitution is desired.

DISCLOSURE OF THE INVENTION

The present invention has been achieved in the light of the aforementioned problems, and it is an object of the invention to provide an interpolation circuit capable of performing interpolation operation with a simple constitution.

The interpolation circuit of the invention comprises oversampling operation unit for performing oversampling operation from the zero-order hold input data, and first convolution operation unit for performing convolution operation on plural data obtained by the oversampling operation unit twice or more repeatedly, characterized in that interpolated data is generated along a quadratic function curve passing through the integral multiples of the value of input data.

Also, the interpolation circuit of the invention comprises oversampling operation unit for performing oversampling operation from the zero-order hold input data, second convolution operation unit for performing convolution operation on plural first data obtained by the oversampling operation unit to calculate plural second data enveloped by a symmetrical trapezoid of the shape having an upside of substantially 0.5 times the width of original input data and a base of substantially 1.5 times the width, and third

convolution operation unit for performing convolution operation on the plural second data obtained by the second convolution operation unit to calculate plural third data enveloped by a smooth quadratic function curve having a width of the base being substantially twice that of the original input data.

Also, the interpolation circuit of the invention comprises oversampling operation unit for performing oversampling operation from the zero-order hold input data, and fourth convolution operation unit for performing convolution operation on plural data obtained by the oversampling operation unit to calculate plural data enveloped by an equilateral triangle having a base being substantially twice the width of original input data.

Also, the interpolation circuit of the invention comprises oversampling operation unit for performing oversampling operation from the zero-order hold input data with a sampling period of $2n \cdot T_1$ at a time interval of T_1, fifth convolution operation unit for performing convolution operation of n phases by adding plural data obtained by the oversampling operation unit n times with the data shifted by the time interval of T_1, and sixth convolution operation unit for performing convolution operation of n phases by adding plural data obtained by the fifth convolution operation unit n times with the data shifted by the time interval of T_1.

In particular, at least one of the fifth and sixth convolution operation unit desirably comprises data holding

unit for holding n pieces of data output from the oversampling operation unit while shifting, and addition unit for adding n pieces of data held in the data holding unit.

In the former stage of the oversampling operation unit, it is desirable to provide data appending unit for appending the data having the symmetrical values proportional to the input data before and after the input data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graph for explaining a principle of interpolation operation that is performed by digital -analog converter of the first embodiment;

FIG. 2 is a graph for explaining a principle of interpolation operation that is performed by digital -analog converter of the first embodiment;

FIG. 3 is a graph for explaining a principle of interpolation operation that is performed by digital -analog converter of the first embodiment;

FIG. 4 is a chart showing a specific example of an interpolation operation;

FIG. 5 is a chart showing a specific example of an interpolation operation;

FIG. 6 is a graph showing a waveform that is finally obtained by arithmetic operations as shown in FIGS. 4 and 5;

FIG. 7 is a diagram showing a waveform corresponding to the partial data shown in FIG. 4;

FIG. 8 is a diagram showing a process for performing the first convolution operation;

FIG. 9 is a diagram showing a process for performing the second convolution operation;

FIG. 10 is a diagram showing a process for performing the third convolution operation;

FIG. 11 is a diagram showing a specific example of the interpolation operation when 0, 3, 7, 5, -4, and 0 are input as the discrete data;

FIG. 12 is a graph showing a waveform that is obtained by arithmetic operation as shown in FIG. 11;

FIG. 13 is a diagram showing the configuration of a digital-analog converter of the first embodiment;

FIG. 14 is a diagram showing the configuration of a digital-analog converter of the second embodiment;

FIG. 15 is a diagram showing a specific example of arithmetic operation in the first, second and third convolution operation circuits included in the digital-analog converter as shown in FIG. 14;

FIG. 16 is a graph showing a waveform that is finally obtained by arithmetic operation as shown in FIG. 15;

FIG. 17 is a diagram showing a waveform with another pulse symmetrically appended on both sides of the single input pulse;

FIG. 18 is a graph showing a result of effecting plural convolution, after appending another pulse of FIG. 17 to the input data;

FIG. 19 is a circuit diagram showing the configuration of a circuit for appending another pulse on both sides of the zero-order hold, single pulse;

FIG. 20 is a graph for explaining the principle of linear interpolation;

FIG. 21 is a circuit diagram showing the configuration of a digital-analog converter for linear interpolation of the fifth embodiment;

FIG. 22 is a diagram showing a specific example of interpolation operation in the case where the discrete input data are 0, 3, 7, 5, -4 and 0; and

FIG. 23 is a graph showing a waveform that is obtained by arithmetic operation as shown in FIG. 22.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of a digital-analog converter to which a data interpolation method of the present invention is applied will be described below with reference to the accompanying drawings.

[First embodiment]

A digital-analog converter in a first embodiment of the invention performs interpolation operation employing a quadratic function curve connecting the input data smoothly when the discrete digital data is input.

FIGS. 1 through 3 are graphs for explaining the principle of interpolation operation that is performed by the digital-analog converter in this embodiment of the invention,

in which the single data is converted into data interpolated along a quadratic function curve. As shown in FIG. 1, the zero-order hold single data is considered to have an amplitude of 1 and a length of $2n \cdot T_1$. When the discrete data is input, the length $2n \cdot T_1$ for the single data is a cycle period (sampling frequency) of input data. For the data as shown in FIG. 1, the first convolution operation is performed by shifting the data by T_1 and performing oversampling operation from the data, and adding the data n times. Consequently, a symmetrical trapezoidal wave with the base of $(3n-1) \cdot T_1$, the upside of $(n+1) \cdot T_1$ and the height of n can be obtained, as shown in FIG. 2. Further, for this symmetrical trapezoidal wave, a second convolution operation is performed by shifting the data by T_1 and adding the data n times, so that a continuous quadratic function curve with the width of $(4n-1) \cdot T_1$ and the amplitude of $2n^2$ can be obtained, as shown in FIG. 3.

In this way, by performing oversampling operation for the zero-order hold input data and then performing convolution operation of n phases, the output data enveloped by the continuous quadratic function curve can be obtained. Therefore, considering a case of zero-order holding the discrete input data successively, the quadratic function curve corresponding to each input data is generated, while being shifted by $2n \cdot T_1$. As a result, the output is 2n pieces of data interpolated along the quadratic function curve passing through and smoothly connecting $2n^2$ times the input data.

FIGS. 4 and 5 are charts showing a specific example of the above mentioned interpolation operation. Herein, a calculation example with n=8 is shown. The detailed contents of the first convolution operation are shown in FIG. 4, and the detailed contents of the second convolution operation are shown in FIG. 5.

In FIG. 4, each item of data listed at (1) is the zero-order hold data (data after oversampling operation) as shown in FIG. 1. The elapse of time is arranged in the transversal direction, the unit of time being T_1 corresponding to one column. Namely, it is supposed that the input data corresponding to FIG. 1 are 16 pieces of zero-order hold data, with the duration of $16T_1$ and an amplitude of 1. An 8-phase convolution operation is performed, comprising producing eight sets of data by shifting the zero-order hold data by time T_1, as shown in (1) through (8) in FIG. 4, and adding them. Consequently, a result of calculation is obtained as listed at (T_1) in FIG. 4. From this result of calculation, it will be found that a symmetrical trapezoidal wave as shown in FIG. 2 is obtained.

In FIG. 5, each item of data listed at (1) is the data obtained by the first convolution operation, and the same as shown at (T_1) in FIG. 4. As listed at (1) through (8) in FIG. 5, an 8-phase convolution operation is performed, comprising producing eight sets of data by shifting the data by time T_1, as shown in (1) through (8) in FIG. 5, and adding them. Consequently, a result of calculation is obtained as listed at (T2) in FIG. 5. (A1) of FIG. 5 is the data obtained by

the second convolution operation, and the same as listed at (T2). A two-phase convolution operation (addition of (A1) data and (A2) data) is performed, comprising shifting the data listed at (A1) by T_1 ((A2) in FIG. 5), so that a result of calculation is obtained as listed at (A3) in FIG. 5.

FIG. 6 is a graph showing a waveform that is finally obtained by arithmetic operations as shown in FIGS. 4 and 5. The longitudinal axis indicates the amplitude, and the transversal axis indicates the time, respectively. As shown in FIG. 6, an original rectangular wave of zero-order hold data results in the oversampled data enveloped by a smooth quadratic function curve with a double width, the maximum amplitude being 128 times ($= 2n^2$).

The above example is described employing the single input data. However, in the case where plural pieces of data are successively input, the data oversampled corresponding to each input data are arranged without overlapping each other. Therefore, when the data is input successively at a period of $2n \cdot T_1$, an interpolation curve always passes through the integral multiple (128 times) of each item of data.

FIG. 7 is a diagram showing a waveform corresponding to the data of (1) in FIG. 4. This waveform corresponds to a zero-order hold unit pulse with an amplitude of 1 and a width of $2n \cdot T_1$. FIG. 8 is a diagram showing a process for performing the first convolution operation, and schematically showing how the amplitude and the width change. Also, FIG. 9 is a diagram showing a process for performing the second convolution

operation, and schematically showing how the amplitude and the width change. FIG. 10 is a diagram showing a process for performing the third convolution operation, and schematically showing how the amplitude and the width change. As shown in FIG. 10, the third convolution operation results in the total width (data length) of plural data after interpolation being $(4n-1)\cdot T_1$.

Then, a continuity test for the waveform obtained by the second convolution operation is made. In FIG. 5, with the position in the transversal direction corresponding to x, the value y of each item of data at (A3) is obtained in the following way.

For $0 \leq x \leq n$, (y in this interval is denoted as y_1)

$$y_1 = (1+2+ \ldots +x)+(1+2+ \ldots +(x-1))$$
$$= x(x+1)/2+(x-1)x/2$$
$$= x^2 \quad \ldots (1)$$

For $n \leq x \leq 3n$, (y in this interval is denoted as y_2)

$$y_2 = 2(1+2+ \ldots +n)-(1+2+ \ldots +(x-n))$$
$$+n(2x-2n-1)$$
$$= n(n+1)-(x-n)^2+n(2x-2n-1)$$
$$= -x^2+4nx-2n^2 \quad \ldots (2)$$

For $3n \leq x \leq 4n$, (y in this interval is denoted as y_3)

$$y_3 = (-x+4n)^2$$
$$= x^2-8nx+16n \quad \ldots (3)$$

In this way, it will be found that y is in a quadratic expression of x.

The inclination at $x = n$ is obtained as follows.

$dy_1/dx = 2x = 2n$

$dy_2/dx = -2x+4n = 2n$

Since both values are equal to 2n, indicating the inclinations at x = n are the same, it will be found that the data is smoothly connected.

Also, the inclination at x=3n is obtained as follows.

$dy_2/dx = -2x+4n = -2n$

$dy_3/dx = 2x-8n = -2n$

Since both values are equal to -2n, indicating that the inclinations at x=3n are the same, it will be found that the data is smoothly connected.

FIG. 11 is a diagram showing a specific example of the interpolation operation when 0, 3, 7, 5, -4, and 0 are input as the discrete data. For example, the specific example is shown in a case of n=4.

As listed at (1) in FIG. 11, first of all, eight zero-order hold oversampled data are generated from the input data. A four-phase convolution operation is performed, comprising generating four sets of data by shifting the eight pieces of input data by time T_1, as listed at (1) through (4) in FIG. 11, and then adding them, whereby a result of calculation can be obtained as listed at (5) in FIG. 11.

Similarly, a four-phase convolution operation is performed, comprising generating four sets of data by shifting the first convolution operation result as obtained in this way by time T_1, as listed at (5) through (8) in FIG. 11, and then adding them, whereby a result of calculation can be

obtained as listed at (A1) in FIG. 11. Then a two-phase convolution operation (addition of (A1) data and (A2) data) is performed, comprising further shifting the data listed at (A1) by T_1 ((A2) in FIG. 11). Consequently, a calculation result is obtained as listed at (A3) in FIG. 11.

FIG. 12 is a graph showing a waveform that is obtained by arithmetic operation as shown in FIG. 11. The longitudinal axis indicates the amplitude, and the transversal axis indicates the time. As shown in FIG. 12, it can be found that the discrete input data is interpolated by the data connect with these data by quadratic function curve. The amplitude of output value corresponding to each input data is 32 times ($=2n^2$) the value of input data.

FIG. 13 is a diagram showing the configuration of a digital-analog converter in this embodiment of the invention. For example, a specific configuration is shown in a case of n=8.

As shown in FIG. 13, the digital-analog converter of this embodiment comprises eight D flip-flops 4 through 11 and an adder (ADD) 12 making up a first convolution operation circuit, eight D flip-flops 13 through 20 and an adder (ADD) 21 making up a second convolution operation circuit, a D flip-flop 22 and an adder (ADD) 23 making up a third convolution operation circuit, a divider 24, a digital-analog converter (D/A) 25, and a filter 26.

A basic clock signal CLK1 has the same frequency as the sampling frequency of the discrete input data, and is input

into an initial stage D flip-flop 4. The discrete input data is fetched into the D flip-flop 4 in synchronism with this basic clock signal CLK1, and held. Also, a clock signal CLK2 has a frequency of 16 times the basic clock signal CLK1. All the D flip-flops at the second stage and beyond perform the operation of sampling the data in synchronism with the clock signal CLK2. The oversampling operation unit is constituted by two D flip-flops 4, 5 into which the clock signals CLK1, CLK2 having different frequencies are input.

If 16-bit data is input into the initial stage D flip-flop 4 in the first convolution operation circuit, seven D flip-flops 5 through 11 at the second stage and beyond accept the data held in this initial stage D flip-flop 4 in synchronism with the clock signal CLK2 in order and successively and shift the data. The adder 12 adds the data held in the eight D flip-flops 4 through 11. In this way, a result of arithmetic operation as listed at (T_1) in FIG. 4 can be obtained in the adder 12 within the first convolution operation circuit.

Also, eight D flip-flops 13 through 20 included in the second convolution operation circuit accept the 19-bit data output from the adder 12 within the first convolution operation circuit in synchronism with the clock signal CLK2 in order and successively and shift the data. The adder 21 adds the data held in the eight D flip-flops 13 through 20. In this way, a result of arithmetic operation as listed at (T2) in FIG. 5 can be obtained in the adder 21 within the second convolution operation circuit.

Further, the D flip-flop 22 included in the third convolution operation circuit accepts the 22-bit data output from the adder 21 within the second convolution operation circuit in synchronism with the clock signal CLK2. The adder 23 adds the data output from the adder 21 and the data held in the D flip-flop 22. In this way, a result of arithmetic operation as listed at (A3) in FIG. 5 can be obtained in the adder 23 within the third convolution operation circuit.

The 23-bit data output from the adder 23 is divided by 8 in the divider 24, and converted into the 20-bit data. This 20-bit data is converted into a stepwise analog signal by the digital-analog converter 25, which is then passed through the filter 26 for suppressing unnecessary radiation by removing a frequency component of 16 times the basic clock signal CLK1, and output.

[Second embodiment]

By the way, in the first embodiment as described above, 2n pieces of zero-order hold data are produced by the oversampling operation on the basis of the input data and shifted by the data interval of T_1, and n sets of shifted data are added. However, the circuit can be simplified by modifying the addition order.

FIG. 14 is a diagram showing the configuration of a digital-analog converter according to a second embodiment of the invention. For example, a specific configuration is shown in a case of n=8.

As shown in FIG. 14, the digital-analog converter of this embodiment comprises nine D flip-flops 31 through 36, 38, 39, and 41 and three adders (ADD) 37, 40, 42 making up a first convolution operation circuit, seven D flip-flops 43 through 46, 48, 49 and 51 and three adders (ADD) 47, 50, 52 making up a second convolution operation circuit, a D flip-flop 53 and an adder (ADD) 54 making up a third convolution operation circuit, a divider 55, a digital-analog converter (D/A) 56, and a filter 57.

Instead of adding eight sets of data that are obtained by shifting eight pieces of zero-order hold data by the data interval T_1, the first convolution operation circuit involves a first addition operation of adding two sets of data shifted by the interval $4T_1$ at a time, a second addition operation of adding two sets of data shifted by the interval $2T_1$ at a time, and a third addition operation of adding two sets of data shifted by the interval T_1.

More specifically, employing four D flip-flops 33 through 36 included in the first convolution operation circuit, the data shifted by $4T_1$ (i.e., four periods of the clock signal CLK2) are generated from eight pieces of zero-order hold data successively input, and the first addition operation of adding the data output from the D flip-flop 32 and the data output from the D flip-flop 36 is performed by the adder 37. Also, employing two D flip-flops 38, 39, the data shifted by $2T_1$ are generated from the data output from the adder 37, and the second addition operation of adding the data output from the

adder 37 and the data output from the D flip-flop 39 is performed by the adder 40. Further, employing the D flip-flop 41, the data shifted by T_1 is generated from the data output from the adder 40, and the third addition operation of adding the data output from the adder 40 and the data output from the D flip-flop 41 is performed by the adder 42. In this way, the same convolution operation is performed in the same manner as the first convolution operation circuit constituted by the eight D flip-flops 4 through 11 and the adder 12 as shown in FIG. 13.

Similarly, employing four D flip-flops 43 through 46 included in the second convolution operation circuit, the data shifted by $4T_1$ are generated from the data output from the adder 42 within the first convolution operation circuit, and the first addition operation of adding the data output from the adder 42 and the data output from the D flip-flop 46 is performed by the adder 47. Also, employing two D flip-flops 48, 49, the data shifted by $2T_1$ is generated from the data output from the adder 47, and the second addition operation of adding the data output from the adder 47 and the data output from the D flip-flop 49 is performed by the adder 50. Further, employing the D flip-flop 51, the data shifted by T_1 is generated from the data output from the adder 50, and the third addition operation of adding the data output from the adder 50 and the data output from the D flip-flop 51 is performed by the adder 52. In this way, the same convolution operation is performed in the same manner as the second convolution operation circuit

constituted by the eight D flip-flops 13 through 20 and the adder 21 as shown in FIG. 13.

Further, the D flip-flop 53 included in the third convolution operation circuit accepts the data output from the adder 52 within the second convolution operation circuit in synchronism with the clock signal CLK2. The adder 54 adds the data output from the adder 52 and the data output from the D flip-flop 53. In this way, the convolution operation is performed by the third convolution operation circuit.

The 23-bit data output from the adder 54 is divided by 8 in the divider 55, and converted into the 20-bit data. This 20-bit data is then converted into a stepwise analog signal by the digital-analog converter 56, which is then passed through a filter 57 for suppressing unnecessary radiation by removing a frequency component of 16 times the basic clock signal CLK1, and output.

FIG. 15 is a diagram showing a specific example of arithmetic operation in the first, second and third convolution operation circuits included in the digital-analog converter as shown in FIG. 14.

In FIG. 15, each item of data as listed at (1) shows the input data from the D flip-flop 32 into the adder 37, and each item of data as listed at (2) shows the data input from the D flip-flop 36 into the adder 37. Also, each item of data as listed at (T_1) and (3) is the same, and is output from the adder 37. Each data as listed at (4) shows the data input from the D flip-flop 39 into the adder 40. Also, each item

of data as listed at (T2) and (5) is the same, and is output from the adder 40. Each data as listed at (6) shows the data input from the D flip-flop 41 into the adder 42. Also, each item of data as listed at (T3) and (7) is the same, and is output from the adder 42. In this way, it will be found that the data ((T3) in FIG. 15) obtained by the first convolution operation circuit is exactly the same as the result of convolution operation as listed at (T_1) in FIG. 4.

Similarly, in FIG. 15, each item of data as listed at (7) shows the data input from the adder 42 into the adder 47, and each item of data as listed at (8) shows the data input from the D flip-flop 46 into the adder 47. Also, each item of data as listed at (T4) and (9) is the same, and is output from the adder 47. Each data as listed at (10) shows the data input from the D flip-flop 49 into the adder 50. Also, each item of data as listed at (T5) and (11) is the same, and is output from the adder 50. Each data as listed at (12) shows the data input from the D flip-flop 51 into the adder 52. Also, each item of data as listed at (T6) and (A1) is the same, and is output from the adder 52. In this way, it will be found that the data ((T6) in FIG. 15) obtained by the second convolution operation circuit is exactly the same as the result of convolution operation as listed at (T2) in FIG. 5.

FIG. 16 is a graph showing a waveform that is finally obtained by arithmetic operation as shown in FIG. 15. The longitudinal axis indicates the amplitude, and the transversal axis indicates the time, respectively. As shown in FIG. 16,

an original rectangular wave of zero-order hold data results in the oversampled data enveloped by a smooth quadratic function curve with a double width, the maximum amplitude being 128 times (= $2n^2$).

In this way, the configuration can be greatly simplified by changing the order of addition. For example, two adders 12, 21 having eight-input are employed in the configuration as shown in FIG. 13, but they can be implemented by seven two-input adders, or a total of 14 adders. On the other hand, six two-input adders 37, 40, 42, 47, 50 and 52 are employed, instead of two eight-input adders 12, 21 in the configuration as shown in FIG. 14, and two adders 12, 21 having eight-input can be removed.

[Fourth embodiment]

By the way, in the above embodiments, the discrete input data is considered to be a single pulse as shown in FIG. 1. However, a pulse with different amplitude and polarity may be symmetrically appended on both sides (fore and back sides) of this single pulse.

FIG. 17 is a diagram showing a waveform with another pulse symmetrically appended on both sides of the single input pulse.

FIG. 18 is a graph showing a result of effecting plural convolution operations on the basis of the operational principle as shown in FIGS. 1 through 3, after appending another pulse of FIG. 17 to the input data. As shown in FIG. 18, a typical interpolation function having positive and negative values can be obtained by performing plural convolution

operations after appending a pulse with different amplitude and polarity on both sides of the single pulse.

FIG. 19 is a diagram showing the configuration of a circuit for appending another pulse on both sides of the zero-order hold, single pulse. A pulse appending circuit (corresponding to data appending unit) as shown in FIG. 19 comprises six D flip-flops 60 through 64, 72, four multipliers 65 through 68, and three adders 69 through 71. An initial stage D flip-flop 60 fetches the data in synchronism with the basic clock signal CLK1 and holds it. Four D flip-flops 61 through 64 connected in tandem operate in synchronism with a clock signal CLK4 having a frequency of one-half the basic clock signal CLK1, to accept the data output from the initial stage D flip-flop 60 in order and successively and hold it. Each output data of the D flip-flop 61, 64 is input into the multiplier 65, 66 having a multiplying factor "-5", respectively. Each output data of the D flip-flop 62, 63 is input into the multiplier with a multiplying factor "31". And the results of multiplication from each of these four multipliers 65 through 68 are added by three adders 69 through 71. In this way, a pulse of FIG. 17 is output from a final stage adder 71. It should be noted that various interpolation functions can be produced by changing the number of stages for the D flip-flop and the multiplying factor or polarity of the multiplier.

[Fifth embodiment]

In the first and second embodiments as previously described, the discrete input data is interpolated between

the data by means of a quadratic function curve. However, the data may be interpolated using the straight line for various purposes.

FIG. 20 is a graph for explaining the principle of linear interpolation. A convolution operation of shifting the zero-order hold data with a length of $2n \cdot T_1$ and an amplitude of 1 as shown in FIG. 1 by T_1 and adding them 2n times, so that an equilateral triangular wave with a base of $(4n-1) \cdot T_1$ and an amplitude of 2n as shown in FIG. 20 can be obtained.

In this way, the output data enveloped by the equilateral triangular wave can be obtained by oversampling the zero-order hold input data 2n times and performing the 2n-phase convolution operation. Accordingly, considering the case of zero-order holding the discrete input data successively, the equilateral triangular wave corresponding to each input data is generated, shifted by $2n \cdot T_1$, and the output data is 2n pieces of data passing through 2n times the input data and connecting them along the equilateral triangular wave.

FIG. 21 is a diagram showing the configuration of a digital-analog converter for linear interpolation in this embodiment. For example, a specific configuration in a case of n=4 is shown.

As shown in FIG. 21, the digital-analog converter of this embodiment comprises eight D flip-flops 81 through 88 and an adder (ADD) 89 making up a convolution operation circuit, a divider 90, a digital-analog (D/A) converter 91, and a filter 92.

If the data is input into an initial stage D flip-flop 81 included in this convolution operation circuit, seven D flip-flops 82 through 88 at the second stage and beyond fetch the data held in this initial stage D flip-flop 81 in synchronism with a clock signal CLK5 (having a frequency of eight times the basic clock signal CLK1) in succession and shift them. The adder 88 adds the data held in eight D flip-flops 81 through 88, respectively. In this way, the convolution operation is performed.

The data output from the adder 88 is divided by 8 in the divider 89, and then converted into a stepwise analog signal by the digital-analog converter 91, which is then passed through a filter 92 for suppressing unnecessary radiation by removing a frequency component of eight times the basic clock signal CLK1, and output.

FIG. 22 is a diagram showing a specific example of interpolation operation in the case where the discrete input data are 0, 3, 7, 5, -4 and 0. For example, a specific example in a case of n=4 is shown.

As listed at (1) in FIG. 22, first of all, eight pieces of zero-order hold data is generated for the input data. An eight-phase convolution operation is performed, comprising generating eight sets of input data by shifting the eight pieces of input data by time T_1, as listed at (1) through (8) in FIG. 22, and then adding them in the adder 89, so that a result of calculation as listed at (T) in FIG. 22 can be obtained.

FIG. 23 is a graph showing a waveform that is obtained by arithmetic operation as shown in FIG. 22. The longitudinal axis indicates the amplitude, and the transversal axis indicates the time. As shown in FIG. 23, it can be found that the discrete input data is interpolated by data connecting with these data by a straight line. The amplitude of output value corresponding to each input data is eight times (=2n) the value of input data. The digital-analog converter as shown in FIG. 22 restores the amplitude to an original value, employing a divider 90.

In the above embodiments, this invention is applied to the digital-analog converter. However, an oversampling circuit may be configured in which an oversampling operation of 2n times the input data is performed by removing the divider, the digital-analog converter and the filter included in each digital-analog converter.

INDUSTRIAL APPLICABILITY

As described above, with this invention, the zero-order hold discrete data can be interpolated with a simple constitution to obtain a smooth waveform or a linearly interpolated waveform. For example, the digital-analog converter of this invention may be replaced with the conventional digital-analog converter used for the digital audio equipment by adding an oscillation circuit with PLL to improve the quality of sound.

Since the interpolated data can be easily generated without referring to the table in the image processing, an extremely wide application range can be considered.

CAIMS

1. An interpolation circuit comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data; and

first convolution operation unit for performing convolution operation on plural data obtained by said oversampling operation unit twice or more repeatedly,

characterized in that interpolated data is generated along a quadratic function curve passing through the integral multiples of the value of said input data.

2. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data;

second convolution operation unit for performing convolution operation on plural first data obtained by said oversampling operation unit to calculate plural second data enveloped by a symmetrical trapezoid of the shape having an upside of substantially 0.5 times a width of original input data and a base of substantially 1.5 times the width; and

third convolution operation unit for performing convolution operation on said plural second data obtained by said second convolution operation unit to calculate plural third data enveloped by a smooth quadratic function curve having the width of a base being substantially twice the width of original input data.

3. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data; and

fourth convolution operation unit for performing convolution operation on plural data obtained by said oversampling operation unit to calculate plural data enveloped by an equilateral triangle having the width of a base being substantially twice the width of said input data.

4. An interpolation circuit, characterized by comprising:

oversampling operation unit for performing oversampling operation from zero-order hold input data with a sampling period of $2n \cdot T_1$ at a time interval of T_1;

fifth convolution operation unit for performing convolution operation of n phases by adding plural data obtained by said oversampling operation unit n times with the data shifted by the time interval of T_1 ; and

sixth convolution operation unit for performing convolution operation of n phases by adding plural data obtained by said fifth convolution operation unit n times with the data shifted by the time interval of T_1.

5. The interpolation circuit according to claim 4, characterized in that at least one of said fifth and sixth convolution operation unit comprises data holding unit for holding n pieces of data output from said oversampling operation unit while shifting, and addition unit for adding n pieces of data held in said data holding unit.

6. The interpolation circuit according to any one of claims 1 through 5, characterized by comprising data appending unit

for appending data having the symmetrical values proportional to the input data before and after said input data in the former stage of said oversampling operation unit.

ABSTRACT

An interpolation circuit capable of performing interpolation operation with a simple constitution. A 16-times oversampling from discrete data is performed by D frip-frops 4, 5. A first convolution operation is performed by D frip-frops 4 through 11 and an adder 12, on the result of which a second convolution operation is performed by D frip-frops 13 through 20 and an adder 21. Data interpolated along a quadratic function curve interpolating the discrete data is obtained from the adder 21.

FIG. 1

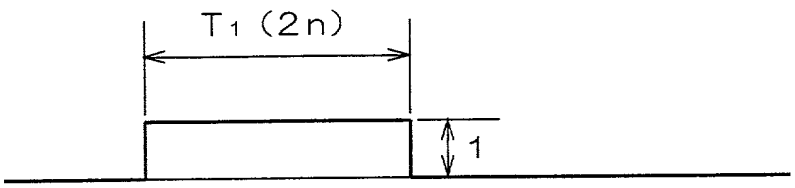


FIG. 2

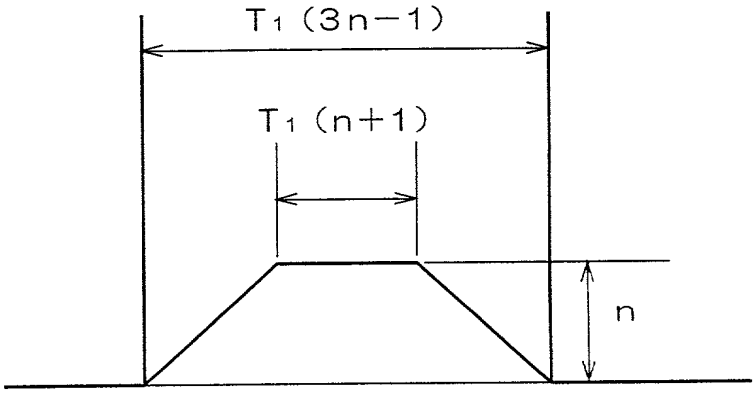


FIG. 3

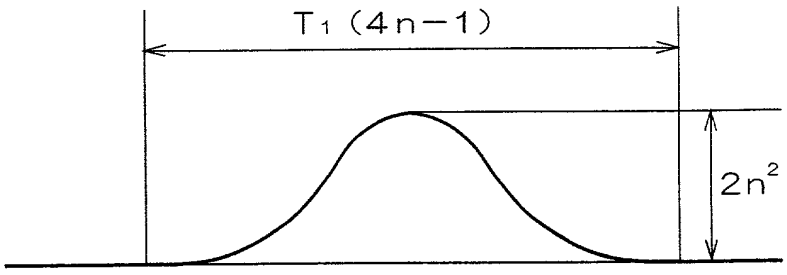


FIG. 4

(1)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
(2)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
(3)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
(4)	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
(5)	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
(6)	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
(7)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
(8)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
(T1)	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1

FIG. 5

(1)	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0	0	0	0	0	0
(2)	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0	0	0	0	0
(3)	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0	0	0	0
(4)	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0	0	0
(5)	0	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0	0
(6)	0	0	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0	0
(7)	0	0	0	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0	0
(8)	0	0	0	0	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	0
(T2)	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1	0
(A1)	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1	0
(A2)	0	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1
(A3)	0	1	4	9	16	25	36	49	64	79	92	103	112	119	124	127	128	127	124	119	112	103	92	79	64	49	36	25	16	9	4	1

FIG. 6

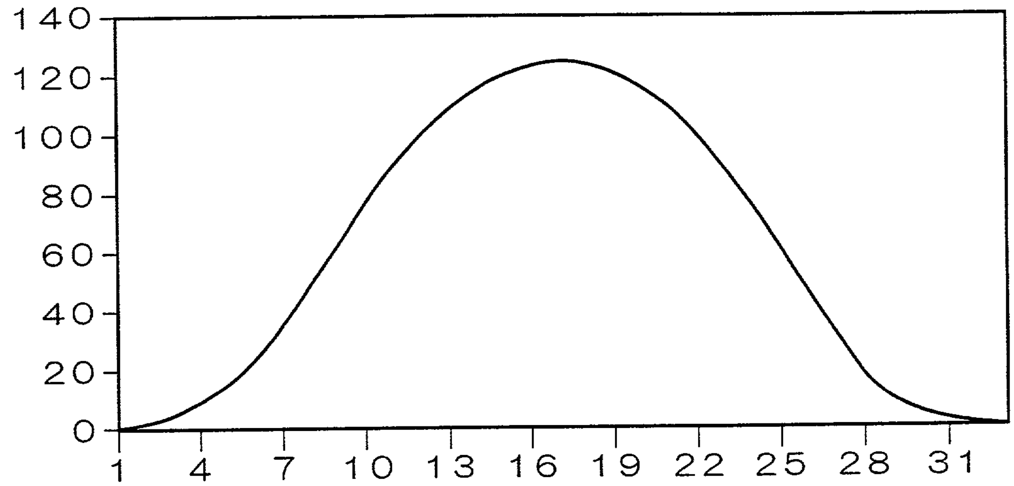


FIG. 7

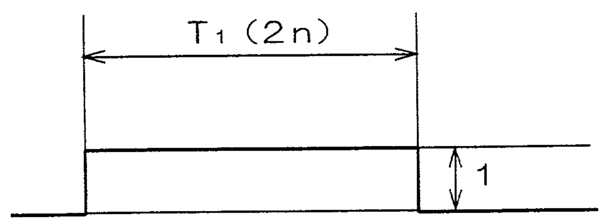


FIG. 8

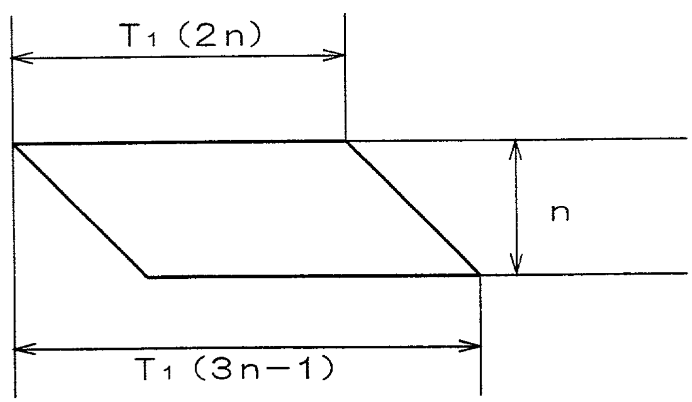


FIG. 9

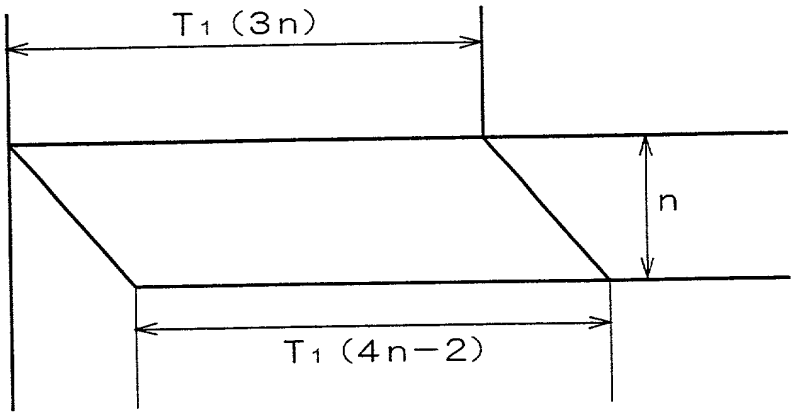
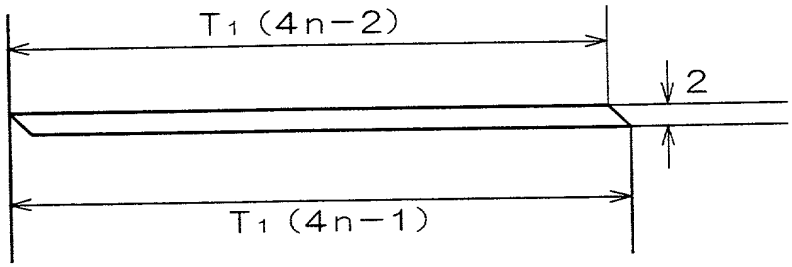


FIG. 10



F/G. 11

(1)	0 0 3 3 3 3 3 3 3 3 7 7 7 7 7 7 7 7 5 5 5 5 5 5 -4 -4 -4 -4 -4 -4 -4 -4 0 0 0 0 0 0 0 0 0 0
(2)	0 0 0 3 3 3 3 3 3 3 3 7 7 7 7 7 7 7 7 5 5 5 5 5 5 -4 -4 -4 -4 -4 -4 -4 -4 0 0 0 0 0 0 0 0 0
(3)	0 0 0 0 3 3 3 3 3 3 3 3 7 7 7 7 7 7 7 7 5 5 5 5 5 5 -4 -4 -4 -4 -4 -4 -4 -4 0 0 0 0 0 0 0 0
(4)	0 0 0 0 0 3 3 3 3 3 3 3 3 7 7 7 7 7 7 7 7 5 5 5 5 5 5 -4 -4 -4 -4 -4 -4 -4 -4 0 0 0 0 0 0 0
(5)	0 0 3 6 9 12 12 12 12 12 16 20 24 28 28 28 28 28 26 24 22 20 20 20 11 2 -7 -16 -16 -16 -16 -16 -12 -8 -4 0 0 0 0
(6)	0 0 0 3 6 9 12 12 12 12 12 16 20 24 28 28 28 28 28 26 24 20 20 20 20 11 2 -7 -16 -16 -16 -16 -16 -12 -8 -4 0 0 0
(7)	0 0 0 0 3 6 9 12 12 12 12 12 16 20 24 28 28 28 28 28 26 20 20 20 20 20 11 2 -7 -16 -16 -16 -16 -16 -12 -8 -4 0 0
(8)	0 0 0 0 0 3 6 9 12 12 12 12 12 16 20 24 28 28 28 28 28 22 20 20 20 20 20 11 2 -7 -16 -16 -16 -16 -16 -12 -8 -4 0
(A1)	0 0 3 9 18 30 39 45 48 48 52 60 72 88 100 108 112 112 110 106 100 82 80 80 71 53 26 -10 -37 -55 -64 -64 -60 -52 -40 -24 -12 -4 0 0
(A2)	0 0 0 3 9 18 30 39 45 48 48 52 60 72 88 100 108 112 112 110 106 86 82 80 80 71 53 26 -10 -37 -55 -64 -64 -60 -52 -40 -24 -12 -4 0
(A3)	0 0 3 12 27 48 69 84 93 96 100 112 132 160 188 208 220 224 222 216 206 168 162 160 151 124 79 16 -47 -92 -119 -128 -124 -112 -92 -64 -36 -16 -4 0

FIG. 12

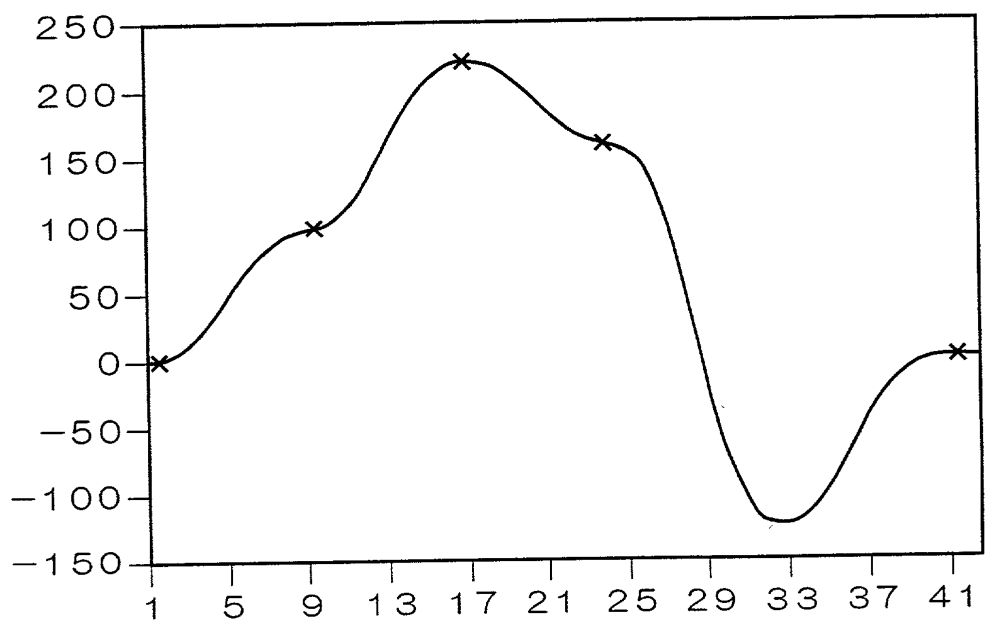


FIG. 13

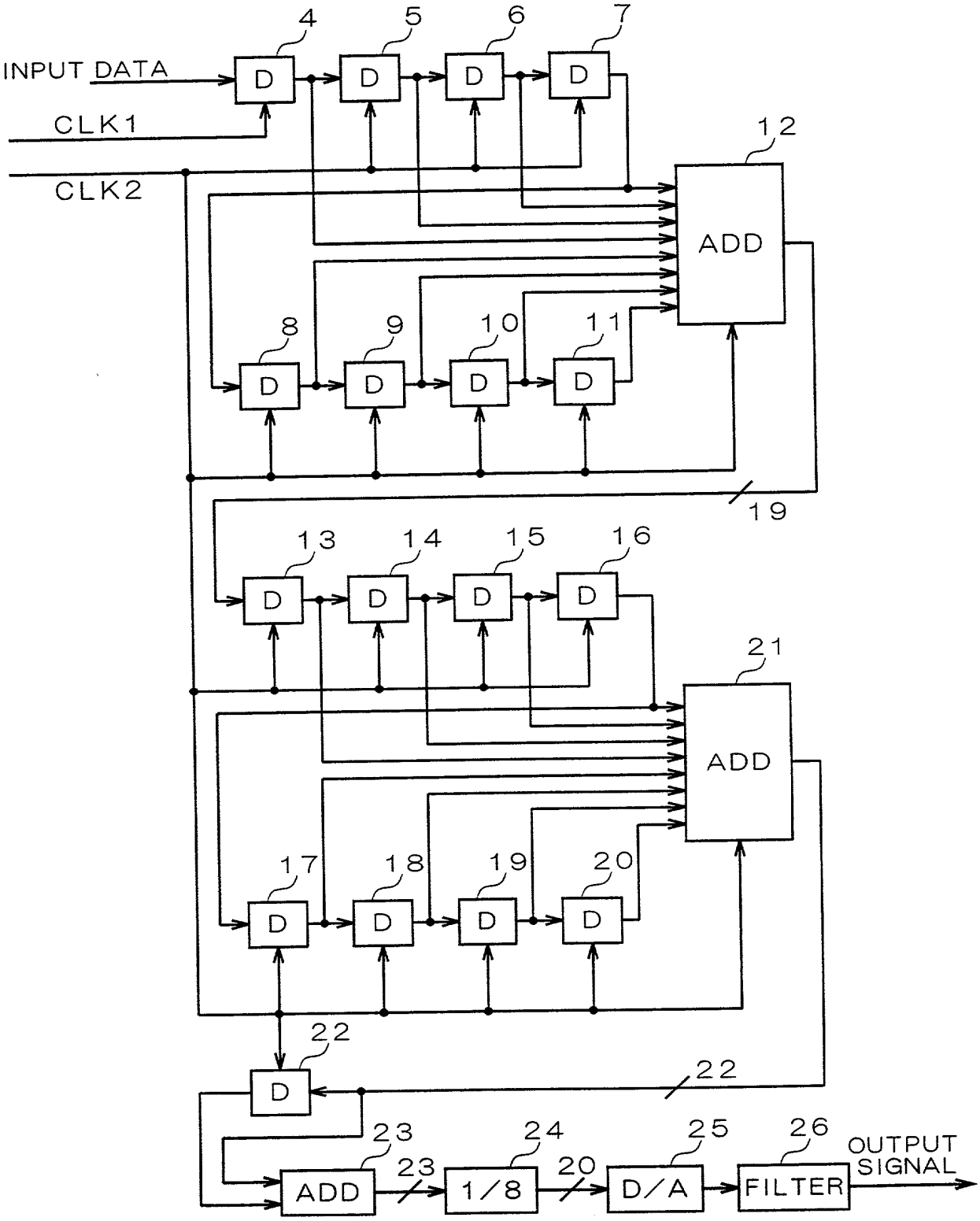

INPUT DATA
CLK1
CLK2
4
5
6
7
D
12
ADD
8
9
10
11
19
13
14
15
16
21
17
18
19
20
22
23
24
25
26
1/8
D/A
FILTER
OUTPUT SIGNAL

FIG. 14

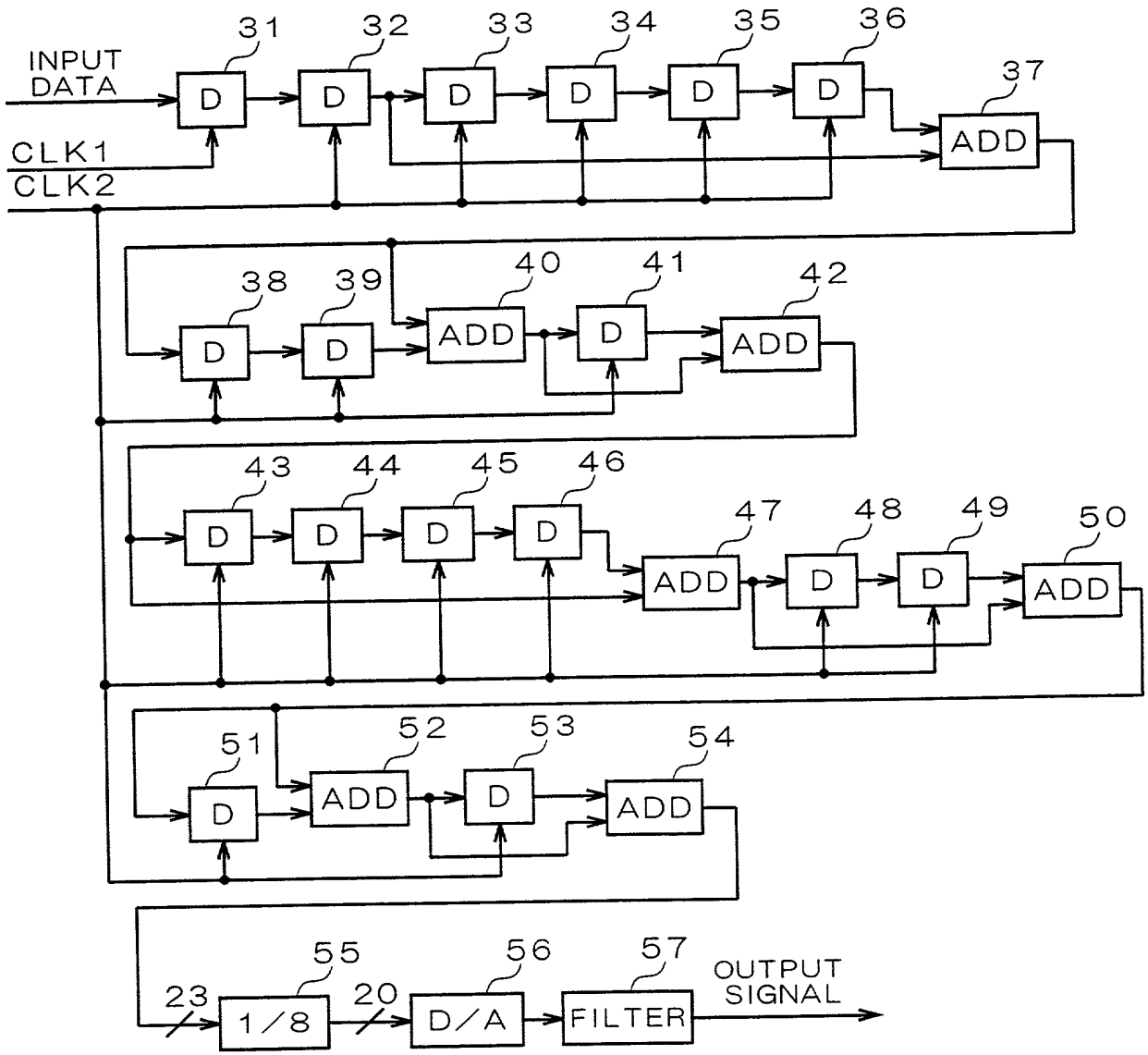

INPUT DATA
CLK1
CLK2
D
ADD
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
23
20
1/8
D/A
FILTER
OUTPUT SIGNAL

FIG. 15

(1)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
(2)	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
(T1)	0	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	1	1	1	1	0	0	0	
(3)	0	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	1	1	1	1	0	0	0	
(4)	0	0	0	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	1	1	1	1	0	
(T2)	0	1	1	2	2	2	3	3	4	4	4	4	4	4	4	4	3	3	2	2	1	1	0	
(5)	0	1	1	2	2	3	3	4	4	4	4	4	4	4	4	4	3	3	2	2	1	1	0	
(6)	0	0	1	1	2	2	3	3	4	4	4	4	4	4	4	4	4	3	3	2	2	1	1	
(T3)	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	
(7)	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	7	6	5	4	3	2	1	
(8)	0	0	0	0	0	1	2	3	4	5	6	7	8	8	8	8	8	8	8	8	7	6	5	
(T4)	0	1	2	3	4	6	8	10	12	13	14	15	16	16	16	16	16	15	14	13	12	10	8	6
(9)	0	1	2	3	4	6	8	10	12	13	14	15	16	16	16	16	16	15	14	13	12	10	8	6	4	3	2	1	0	0	0
(10)	0	0	0	1	2	3	4	6	8	10	12	13	14	15	16	16	16	16	16	15	14	13	12	10	8	6	4	3	2	1	0
(T5)	0	1	2	4	6	9	12	16	20	23	26	28	30	31	32	32	32	31	30	28	26	23	20	16	12	9	6	4	2	1	0
(11)	0	1	2	4	6	9	12	16	20	23	26	28	30	31	32	32	32	31	30	28	26	23	20	16	12	9	6	4	2	1	0	0
(12)	0	0	1	2	4	6	9	12	16	20	23	26	28	30	31	32	32	32	31	30	28	26	23	20	16	12	9	6	4	2	1	0
(T6)	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1	0
(A1)	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1	0	0
(A2)	0	0	1	3	6	10	15	21	28	36	43	49	54	58	61	63	64	64	63	61	58	54	49	43	36	28	21	15	10	6	3	1	0
(A3)	0	1	4	9	16	25	36	49	64	79	92	103	112	119	124	127	128	127	124	119	112	103	92	79	64	49	36	25	16	9	4	1	0

FIG. 16

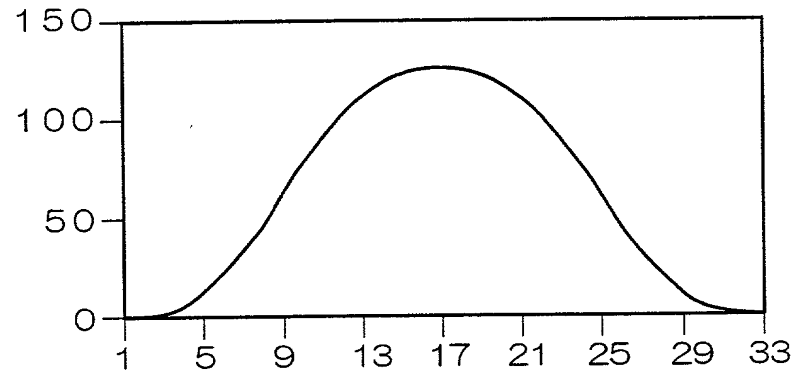


FIG. 17

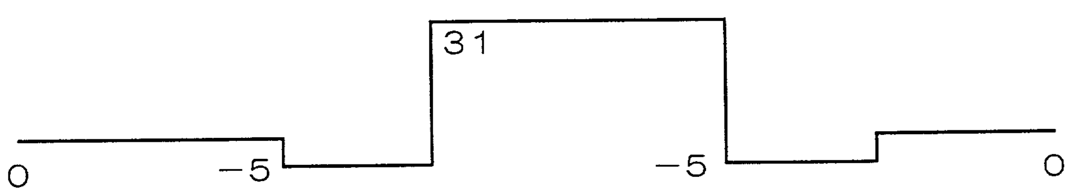


FIG. 18

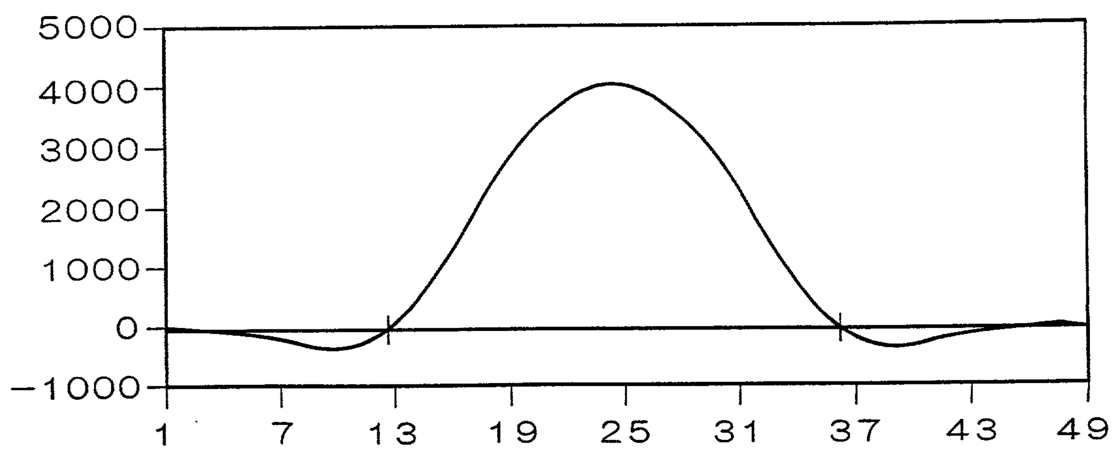


FIG. 19

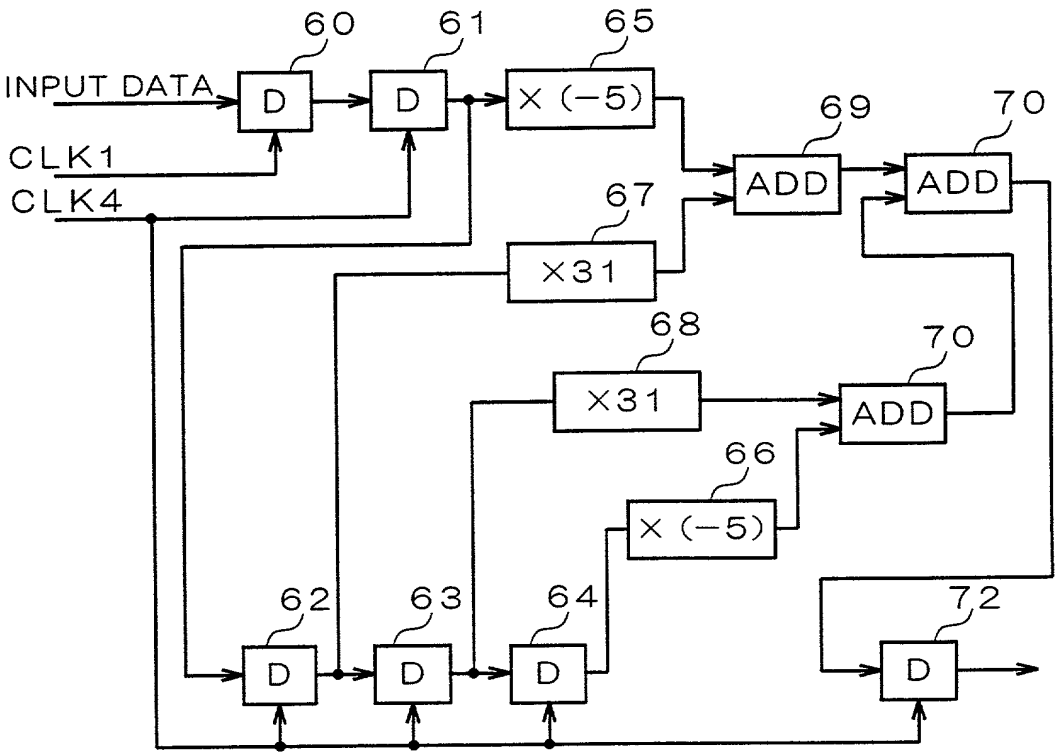

60
61
65
INPUT DATA
D
D
X (−5)
69
70
CLK1
CLK4
ADD
ADD
67
X31
68
70
X31
ADD
66
X (−5)
62
63
64
72
D
D
D
D

FIG. 20

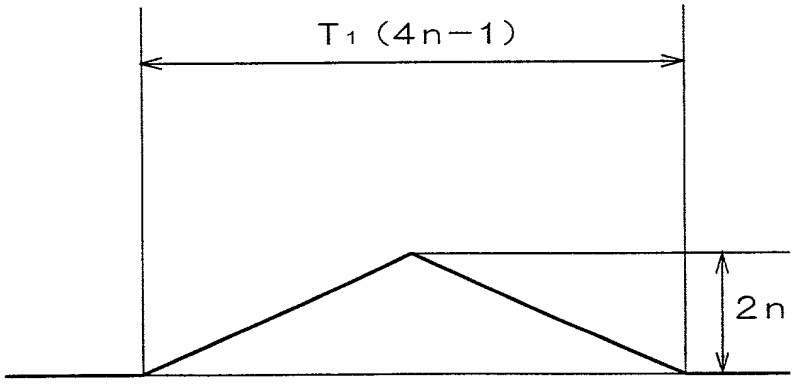

T1 (4n−1)
2n

FIG. 21

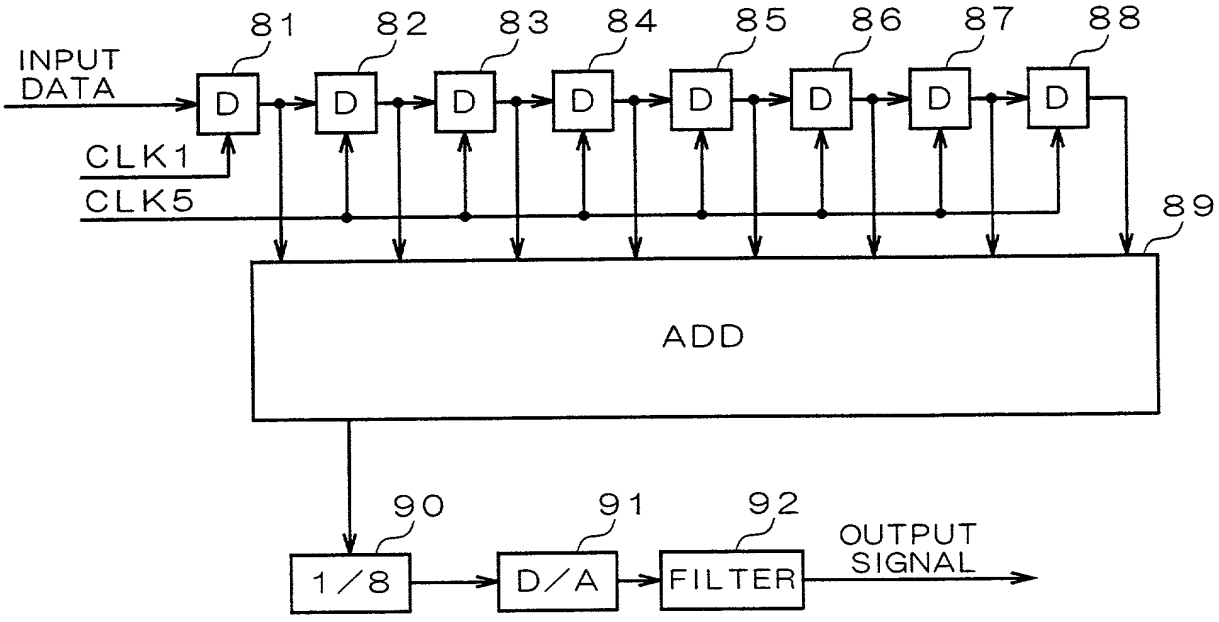
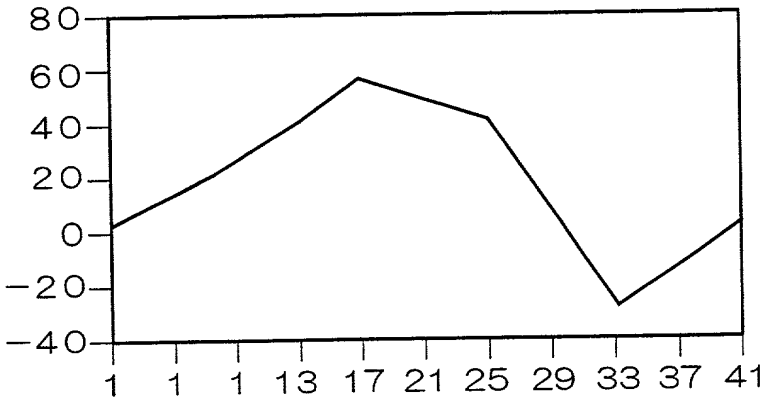


FIG. 22

(1)	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0	0	0	0	0	0
(2)	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0	0	0	0	0
(3)	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0	0	0	0
(4)	0	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0	0	0
(5)	0	0	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0	0
(6)	0	0	0	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0	0
(7)	0	0	0	0	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0	0
(8)	0	0	0	0	0	0	0	0	3	3	3	3	3	3	3	3	7	7	7	7	7	7	7	7	5	5	5	5	5	5	5	5	-4	-4	-4	-4	-4	-4	-4	-4	0	0	0
(T)	0	3	6	9	12	15	18	21	24	28	32	36	40	44	48	52	56	54	52	50	48	46	44	42	40	31	22	13	4	-5	-14	-23	-32	-28	-24	-20	-16	-12	-8	-4	0	0	0

FIG. 23



Docket No.
A-401

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

INTERPOLATION CIRCUIT

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on **11 May 2000** as United States Application No. or PCT International Application Number **PCT/JP00/03040**

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
11-165745	**JAPAN**	**11 May 1999**	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James H. Walters, Reg. No. 35,731

I authorize the attorney that I have appointed to accept instructions regarding this application and the resulting patent from Amagai Patent Firm.

Send Correspondence to: **Customer No. 802**
DELLETT AND WALTERS
310 S.W. Fourth Avenue, Suite 1101
Portland, Oregon 97204 US

Direct Telephone Calls to: *(name and telephone number)*
James H. Walters (503) 224-0115

Full name of sole or first inventor **Yukio Koyanagi**
Sole or first inventor's signature 小柳 裕喜生 Date August 24, 2001
Residence **Yamanashi, JAPAN** JPY
Citizenship **JAPAN**
Post Office Address **63-1-205 Isawa-chou, Higashiyatsushiro-gun, Yamanashi**
406-0000 JAPAN

Full name of second inventor, if any
Second inventor's signature Date
Residence
Citizenship
Post Office Address